22. (Amended) The method of Claim 16, wherein n-doped or p-doped areas for the creation of the structures forming the semiconductor components are produced in the active areas.

25. (Amended) The method of Claim 1 employed for the creation of a structure forming a photosensitive transistor in which an n-doped area is implanted into the p-doped inner area, whereby the terminal forming the collector at the fringe area of the n-doped trough and the terminal forming the emitter at the n-doped area implanted into the p-doped inner area is created.

26. (Amended) The method of Claim 1, wherein the p-doped or the n-doped semiconductor substrate is a weakly p-doped or n-doped semiconductor substrate.

PCT ARTICLE 19 AMENDMENT

CHANGED PATENT CLAIMS

[Received at the International Bureau on March 13, 2000 (13.03.00); Original Claim 1 changed; all other Claims remain unchanged (1 page)]

1. A method for producing integrable semiconductor components, in particular transistors, diodes, and logic gates, starting with a p-doped or n-doped semiconductor substrate in the following steps:

   application of a mask onto the semiconductor substrate for definition of a window delimited by a peripheral edge;

   production of an n-doped trough in the p-doped semiconductor substrate or p-doped trough in the n-doped semiconductor substrate by means of ion implantation through the mask using an energy that will assure that a p-doped or an n-doped inner area remains on the surface of the semiconductor substrate, whereby the fringe area of the n-doped or p-doped trough extends up to the surface of the semiconductor substrate, and

   production of additional n-doped and/or p-doped areas in the p-doped or n-doped inner area and in the fringe area of the n-doped or the p-doped trough form the structure of the semiconductor component.

2. The method of Claim 1 wherein, for creation of the structure forming an NPN-transistor, a p-doped area having heavier doping than that of the semiconductor substrate together with the p-doped area enclosed by the p-doped inner area forming the base of the transistor and an n-doped area forming the emitter of the transistor